6.6 A 1.2V 240MHz CMOS Continuous-Time Low-Pass Filter for a UWB Radio Receiver

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An integrated 5th-order 0.13µm CMOS G_m-C low-pass filter for the WiMedia UWB system [1] is presented. It is targeted for a direct-conversion receiver, which in a UWB system results in a filter corner frequency requirement of 240MHz. A 5th-order prototype is selected to suppress interference from concurrently operating radio transmitters in the vicinity of or within the same terminal [2]. For example, cellular or WLAN transmitters can interfere with a UWB receiver. The filter uses a 1.2V supply voltage and includes an adjustable gain control from 13dB to 48dB in 1dB gain steps. In addition to the G_m-C filter, the implemented circuit consists of an output buffer designed to drive a 5b analog-to-digital converter (ADC) [3] and a current-steering digital-to-analog converter (DAC) for DC-offset compensation, as shown in Fig. 6.6.1.

The conventional approach to G_m-C filters is to design the transconductors with a sufficiently high bandwidth and DC gain, thus mitigating their effect on the filter frequency response. However, the extreme bandwidth required from the transconductors combined with the 1.2V supply voltage of 0.13µm CMOS make it difficult to simultaneously realize a high DC gain. The approach proposed here is to accept a low DC gain for the transconductors, but to take into account the loss already in the filter synthesis. This enables the use of a simple transconductor circuit which has no internal bandwidth limitation. Although the DC gain can be low, it must be accurate with a precision dependent on the Q values of the filter poles and the DC gain itself [4]. The filter is synthesized for a transconductor DC gain of 24dB. The resulting accuracy requirement with this gain is 1dB for a 0.3dB amplitude error at the passband edge. In the synthesis, the resistive load of the LC prototype and the related transconductor are eliminated to allow for higher loss in the transconductors. The filter is implemented as a cascade of a real pole placed at the filter input and a 4th-order leapfrog G_m-C filter, which realizes the complex pole pairs of the transfer function. The real pole is implemented with passive components thus improving the out-of-band linearity compared to an active implementation.

The core of the transconductor used in the filter is a pseudo-differential structure with NMOS input transistors and PMOS current source loads. Considering the low supply voltage, the lack of cascode and tail transistors it is important to increase the output voltage range and to minimize the noise from the PMOS transistors. The complete transconductor, shown in Fig. 6.6.2, combines common-mode feedforward (CMFF) and feedback (CMFB) to obtain input common-mode rejection and to establish a common-mode (CM) level at the transconductor output. The CMFF replicates the common-mode current and subtracts it from the transconductor output. The CMFB circuit reuses the common-mode signal generated by the CMFF of the following transconductor. In [5], an almost identical transconductor has a CMFB circuit referring to the CM-level at the transconductor input, thus effectively canceling any common-mode rejection realized with CMFF. Here a CM-reference signal is introduced via transistor M5, leading to DC common-mode rejection being limited by the accuracy of the PMOS current mirror in the CMFF circuit.

The CMFF circuit introduces a small CM current to transconductor output due to a systematic error in the PMOS current mirror. However, the CMFB is unable to adequately suppress the error leading to a shift in the output CM voltage. The CM error is accumulated in the filter due to the high voltage gain and since the transconductor G_ms are dependent on the input CM level, the filter frequency response is deteriorated. These systematic CM-level errors are cancelled by a bias circuit adding the CM error with reverse polarity to the CM-reference signal used by transconductors. The DC gain of the transconductors is stabilized with a tunable negative resistance circuit, shown in Fig. 6.6.3, which is connected to the transconductor output. The tuning of the negative resistance and consequently the DC gain is accomplished by controlling the V_{GS} of the degeneration transistors.

The 48dB voltage gain is partitioned between the first three filter stages and the output buffer. The gain control is divided into 6dB and 1dB steps implemented in the filter input transconductor and output buffer, respectively. The 6dB steps are implemented by dividing the input transconductor into six parallel transconductors whose inputs can be individually disconnected from the leapfrog filter input with CMOS switches as shown in Fig. 6.6.4. Dummy transconductors, biased at zero current, are switched in place of the actual transconductors to keep the passive pole frequency unchanged. The outputs of the disconnected transconductors remain connected to the filter, while their inputs are connected to a bias voltage to keep the source impedance seen by the rest of the filter unaffected. The 1dB steps are accomplished by switching the resistive load of the output buffer.

The corner frequencies of the passive pole and the ladder filter are controlled separately by 5b switched-capacitor matrices. Separate controls are required, since the leapfrog filter corner frequency is proportional to the G_m of the transconductors, while the passive pole frequency is dependent on the source resistance, which is the load of the preceding mixer. The capacitor matrices utilize differential NMOS switches for high Q and small NMOS transistors for biasing. The width of the differential switches is maximized considering the required tuning range. The simulated Q is 280 which causes negligible error in the frequency response.

The filter is fabricated in a 0.13µm CMOS process and the chips are bonded directly to a PCB. The micrograph of the implemented filter is shown in Fig. 6.6.5. The filter includes an input test buffer for measurement purposes. The frequency response and the linearity are measured using a test output while the voltage gain and the noise are measured using a 5b ADC [3]. The measured performance results are summarized in Fig. 6.6.6. The measured and simulated frequency responses of the filter are shown in Fig. 6.6.7. The passband edge frequency is 240MHz and the measured frequency response is scaled to 0dB at 10MHz. The integrated input-referred noise is $117\mu V_{rms}$, corresponding to 7.7nV/√Hz noise density. The noise is integrated from 2 to 233MHz, which is the downconverted UWB channel occupying all the subcarriers. The filter consumes 24mW and both the filter gain control as well as the DC gain adjustment of the transconductors operate correctly. Assuming a 30dB voltage gain for the RF front-end, the demonstrated filter performance implemented in deep-submicron CMOS leads to negligible deterioration of receiver dynamic range despite the high level of functionality and selectivity.

Acknowledgements:
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References:
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[2] J. Bergervoet, K. Harish, G. van der Weide, et al., "An Interference Robust Receive Chain for UWB Radio in SiGe BiCMOS," *ISSCC Dig. Tech. Papers*, pp. 200-201, Feb., 2005.
[3] O. Viitala, S. Lindfors, and K. Halonen, "A 5-Bit 1GS/s Flash-ADC in 0.13-µm CMOS Using Active Interpolation," *Proc. ESSCIRC*, pp.412-415, Sept., 2006.
[4] A. Baschirotto, R. Alini, and R. Castello, "BiCMOS Operational Amplifier with Precise and Stable DC Gain for High-Frequency Switched Capacitor Circuits," *Electronics Letters*, vol. 27, no. 15, pp. 1338-1340, July, 1991.
[5] P. Kallam, E. Sanchez-Sinencio, and A.I. Karsilayan, "An Enhanced Adaptive Q-Tuning Scheme for a 100-MHz Fully Symmetric OTA-Based Bandpass Filter," *IEEE J. Solid-State Circuits*, vol. 38, pp. 585-593, April, 2003.

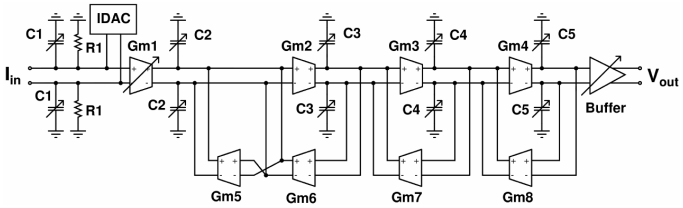

Figure 6.6.1: Block diagram of the implemented filter.

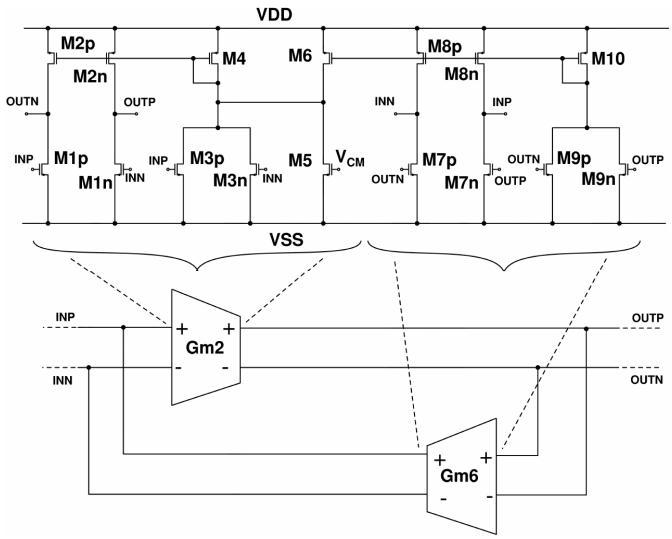

Figure 6.6.2: Transconductor with CMFF and CMFB circuit.

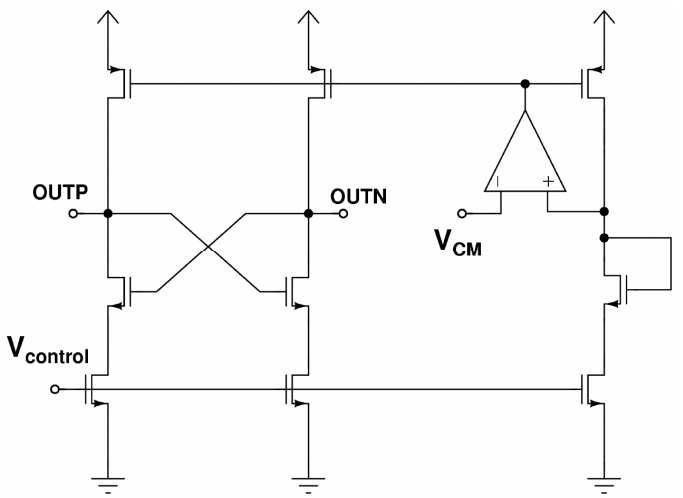

Figure 6.6.3: Negative-resistance circuit.

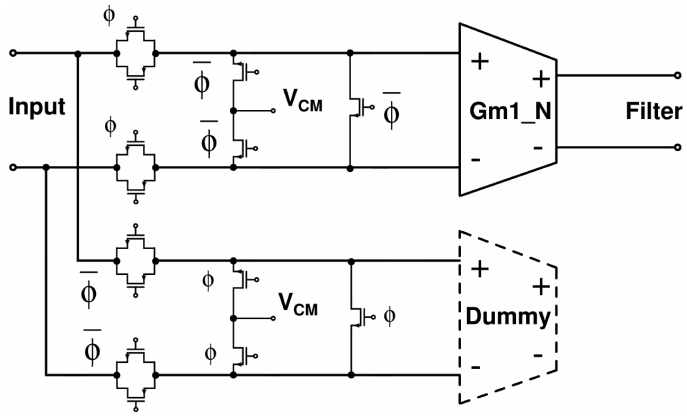

Figure 6.6.4: Gain control slice from the input transconductor G_{m1}.

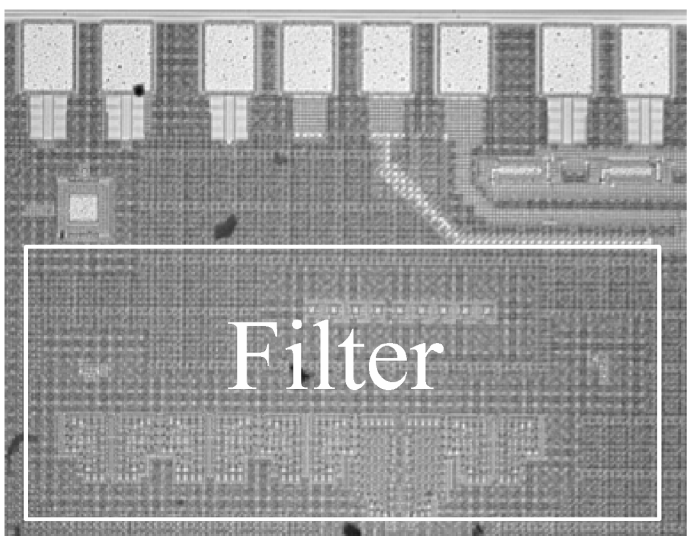

Figure 6.6.5: Die micrograph.

Technology	0.13μm CMOS
Filter order	5
Supply voltage	1.2V
Voltage gain at 10MHz	12.9 to 47.6dB
Passband edge frequency	240MHz
Integrated input-referred noise (2 to 233MHz)	117μV_{rms}
Input-referred noise density	7.7nV/√Hz
IIP3 (in-band, f_1 =30 MHz, f_2 = 50MHz)	−48.2dBV
IIP3 (out-of-band, f_1 = 400MHz, f_2 = 790MHz)	−8.2dBV
IIP2 (out-of-band, f_1 = 410MHz, f_2 = 400MHz)	+18.2dBV
Power consumption	24mW
Die area without pads	0.34mm^2

Figure 6.6.6: Measured performance.

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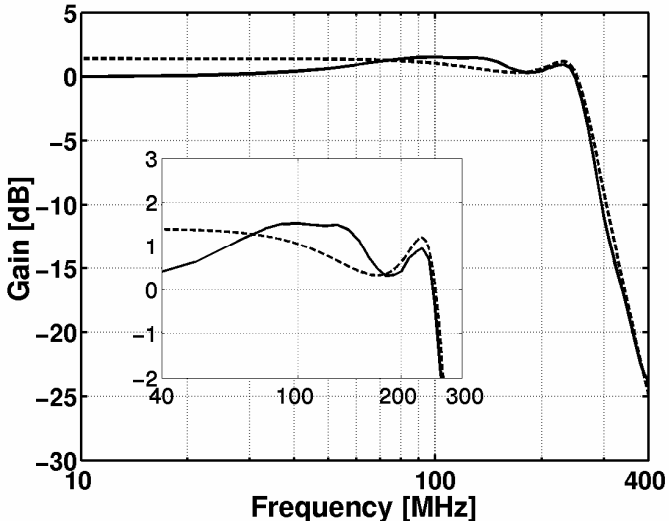

Figure 6.6.7: Measured (solid line) and simulated (dashed line) frequency responses.

